REMARKS

The Office Action dated July 22, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1-8 are pending in the present application, and claims 5-8 are respectfully submitted for consideration.

Allowed Claims 1-4

As a preliminary matter, Applicants appreciate the allowance of claims 1-4.

Formal Matter

Claim 6 was rejected under 35 U.S.C. § 112, first paragraph because the Examiner took the position that the specification "while being enabling for constructing the clock switching circuit with the PLL circuit and flip-flop groups in the claimed structure, does not reasonably provide enablement for preventing the clock switching circuit from producing a hazard by the ratio between the numbers of the flip-flop groups." The Examiner further noted that "the claim language merely states that the number of the second flip-flop group is greater than the number of the first flip-flop group ... [and] does not enable one on how much greater and what the number of the second flip-flop group has to be in order to prevent the so-called hazard." (See page 2 of Office Action)

Applicants respectfully disagree with the Examiner position, and therefore traverse the rejection. It is submitted that the written description of the present application is in full, clear, concise, and exact terms to enable a person skilled in the art

to make and use the present invention in accordance with 35 U.S.C. § 112, first paragraph.

Specifically, Applicants submit that the specification of the present application provides a full and clear disclosure to enable a person skilled in the art to determine "how much greater and what the number of the second flip-flop group has to be in order to prevent the ... hazard." For instance, page 13, lines 10-16 of the specification provides,

> A second flip-flop group 45 comprises more stages of flip-flops F/F than the first flip-flop group 43. This difference in number of stages is set according to the difference in frequencies of the first clock X'tal and the second clock PLL. In the example shown in Fig. 5, the second flip-flop group 45 comprises 2N stages of flip-flops F/F(1a)(1b) to F/F(Na)(Nb). (Emphasis Added.)

In addition to the passage above, Figure 5 of the drawings clearly shows an exemplary embodiment of a circuit diagram of a clock switching circuit of the present invention having a First Flip-Flop Group 43 and a Second Flip-Flop Group 45, where the Second Flip-Flop Group 45 includes flip-flops F/F(1a)(1b) to F/F(Na)(Nb). Hence, Applicants submit that present application provides a full and clear disclosure to enable a person skilled in the art to determine "how much greater and what the number of the second flip-flop group has to be in order to prevent the ... hazard."

Thus, Applicants respectfully submit that claim 6 is allowable and request withdrawal of the rejection.

Claims 5, 7-8 Recite Patentable Subject Matter

Claim 5 was rejected under 35 U.S.C. § 102(b) as being anticipated by Yokogawa et al. (U.S. Patent No. 4,872,155, "Yokogawa"). Applicants respectfully traverse the rejection and submit that claim 5 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 5 recites a method for controlling a clock switching circuit comprising, among other features, the step of receiving a PLL clock signal ... said PLL clock signal being faster than the basic clock, and counting a number of the PLL clock signal after inhibiting outputting the basic clock signal, and outputting the PLL clock signal after the number of the PLL clock signal which is a predetermined number.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

The Office Action characterized Yokogawa as allegedly disclosing, "counting the clock signal number, inhibiting the clock output, and output PLL clock signal after a predetermined number of clock signals (column 4, lines 59-64, column 5, lines 4-6)." Furthermore, the Office Action noted that, "the prior art discloses a counter receiving an detecting the pulse spacing of the clock data (column 4, lines 59-61), which is the claimed counting a number of the basic clock signal after inhibiting outputting the basic clock signals. The prior art further discloses a supply circuit for supplying the PLL circuit with the signal after the predetermined number of clock signals (column 4, lines 62-64) for the PLL circuit to output the synchronized signal (column 5, lines 4-6)."

Applicants respectfully disagree with the Examiner's characterization of Yokogawa. In particular, Column 4, lines 59-64 of Yokogawa merely states, in part, the following:

> ...a counter detecting the pulse spacing of the clock data or a signal synchronized with the clock data by counting the clock pulses, and a supply circuit for supplying the PLL circuit with a signal corresponding to the count value of the counter.

Column 5, lines 4-6 of Yokogawa states, in part, the following:

> The PLL circuit generating the clock in synchronism with the clock data is constructed of these circuits.

It is clear from the cited passages above that Yokogawa fails to show at least a PLL clock signal that is faster than the basic clock, and the counting of a number of the PLL signal after inhibiting outputting the basic clock signal. In fact, Yokogawa is completely silent regarding the above features of the present invention, especially in the passages cited by the Examiner. Therefore, Applicants submit that Yokogawa fails to disclose each and every element recited in claim 5 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Yokogawa fails to disclose or suggest each and every feature of claim 5. Accordingly, Applicants respectfully submit that claim 5 is not anticipated by nor rendered obvious by the disclosure of Yokogawa. Therefore, Applicants respectfully submit that claim 5 is allowable.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Claims 7-8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Parmenter et al. (U.S. Patent No. 5,679,353, "Parmenter"). Applicants respectfully traverse the rejection and submit that each of claims 7 and 8 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 7 recites a clock signal switching circuit that switches an output from a basic clock to a fast clock comprising, among other features, an inhibiting circuit that inhibits said fast clock by a time when said basic clock disappears in said output in the case of switching said output from said clock to said fast clock.

Claim 8 recites a clock signal switching circuit that switches an output from a basic clock to a fast clock comprising, among other features, an inhibiting circuit that inhibits said fast clock within a term which depends on a difference between said frequency of said basic clock and said frequency of said fast clock in the case of switching said output from said basic clock to said fast clock.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Parmenter discloses a dynamic clock mode switch (11) provided for switching clock frequencies while allowing continuing operation of a depending system. The switch (11) includes an enable circuit for transmitting an enable signal, a phase-locked loop circuit (PLL) (15) for locking onto an input clock frequency in response to said enable circuit, a PLL lock indicator for receiving a PLL lock signal (29) from said PLL, and a clock multiplexer with a multiplier for multiplying said input clock frequency by a predetermined factor in response to said enable circuit and PLL clock signals.

The Examiner characterized the clock multiplexers 19 and 21 of Parmenter as being the inhibiting circuit of the claimed invention. However, Applicants submit that the clock multiplexers 19 and 21 of Parmenter, taken together or individually, is neither comparable nor analogous to the inhibiting circuit of the present invention. In fact, Parmenter merely shows multiplexers 19, 21 receiving a second input signals 2X_CLK2 and 1X_CLK2 respectively. The multiplexers 19, 21 of Parmenter are activated by logic circuitry node 27 where the logic circuitry 13 receives as input the output from node 23, feedback signal from node 25, CKD enable signal and a PLL lock signal from line 29. Upon enablement, multiplexers 19 and 21 send output signals to divider circuitries 3, 33, respectively. It is submitted that Parmenter is completely silent on "an inhibiting circuit that inhibits said fast clock by a time when said basic clock disappears in said output in the case of switching said output from said clock to said fast clock" as well as "an inhibiting circuit that inhibits said fast clock within a term which depends on a difference between said frequency of said basic clock and said frequency of said fast clock in the case of switching said output from said basic clock to said fast clock." Therefore, Applicants submit that Parmenter fails to disclose each and every element recited in claims 7 and 8 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Parmentor fails to disclose or suggest each and every feature of claims 7 and 8. Accordingly, Applicants respectfully submit that claims 7 and 8 are not

anticipated by nor rendered obvious by the disclosure of Parmenter. Therefore, Applicants respectfully submit that claims 7 and 8 are also allowable.

Accordingly, Applicants respectfully request withdrawal of the rejection.

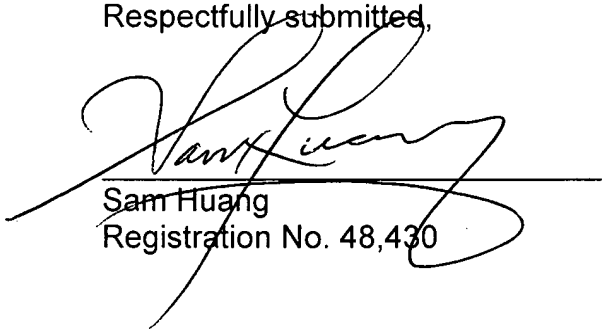
Conclusion

In view of the above, Applicants respectfully submit that each of claims 5-8 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 5-8 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108066-00018.

Respectfully submitted,



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Enclosure: Petition for Extension of Time (3 months)